

**FACSIMILE TRANSMISSION**

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Our ref: MIO 0042 V2

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Applicants : John D. Porter and William N. Thompson  
Serial No. : 09/740,174  
Filed : December 18, 2000  
Title : LATCH-UP PREVENTION FOR MEMORY CELLS  
Docket No : MIO 0042 V2  
Examiner : M. Trinh  
Art Unit : 2822  
Confirm. No.: 5372

  
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## OFFICIAL RESPONSE

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of

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## CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this correspondence is being facsimile transmitted to the Patent and Trademark Office at fax no. ((202) 303-3453) on December 19, 2002.

Thomas E. Lees

46,867  
Reg. No.SUPPLEMENTAL AMENDMENT

This paper is being filed in response to the Office action mailed December 12, 2002 having a one month reply due date of January 12, 2003.

IN THE CLAIMS

Amended claims are indicated as such in the parenthetical following the claim number.

Further, enclosed herewith is a separate paper entitled "Version With Markings To Show Changes Made" which corresponds to the amendments to the claims made herein.

Please amend claims 43-50.

43. (Amended) A method of fabricating a memory cell comprising:

- providing a substrate;
- forming a first semiconductor structure and a second semiconductor structure within the substrate;
- forming a first pull-up transistor having a first source and a first drain in the first semiconductor structure and a first gate over the first semiconductor structure;
- forming a first pull-down transistor having a second source and a second drain in the substrate and a second gate over the substrate;
- forming a first contact and a second contact within the first semiconductor structure;

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